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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,254	GROEN ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) *2,7,17 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) *1,3-5,8,9 and 23* is/are allowed.

6)☒ Claim(s) *1, 3-6, 8-16, 18-23* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see "Remarks", filed 4/10/08, with respect to the rejection(s) of independent claim(s) 1, 6, 8, 10, 14, 19, 22, 23 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection of independent claims 1, 6, 8, 10, 14, 19, 22, 23 is made in view of Mahajan et al. (U.S. 6,618,358).

Claim Objections

2. Claims 11-12 are objected to because of the following informalities: Claims 11,12 line 3 both recite: "...by the programmable logic fabric portion..." referring to claim 10, but claim 10 does not recite "a programmable logic fabric portion".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-6, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahajan et al. (U.S. 6,618,358) in view of Peace (U.S. 6,687,260) and Hashiguchi (U.S. 5,987,540).

With respect to claim 1, Mahajan et al. disclose: first clock data recovery circuitry for receiving first data and recovering a first recovered clock form the first data (Fig. 2, block 210 receiving data T1 and outputting recovered clock signal CLK1, see column 4, lines 12-22); a second clock data recovery circuitry for receiving second data and recovering a second recovered clock from the second data (Fig. 2, block 220 CLK2 is the second recovered clock column 4, lines 12-22); wherein the transceiver (Fig. 2 the network access server 250, that transmits and receives data, functions as a transceiver, see column 1, lines 19-20) provides the first recovered clock, the second recovered clock, the first data and the second data to a clock based functionality of the transceiver (clock based functionality comprises blocks 252, 254 and the circuit which receives the selected clock see column 1, lines 58-65, the selected clock is used for subsequent processing, as a data transfer clock for example); and wherein the clock based functionality chooses among the first recovered clock, the second recovered clock, and the reference clock for subsequent processing (column 1, lines 59-65, the selected clock is used as a data transfer clock in a switch).

Mahajan et al. do not expressly teach: serial data; a plurality of clock based functionalities; each of the plurality of clock based functionalities chooses among the first recovered clock, the second recovered clock, and the reference clock for subsequent processing of one of the first serial and the second serial data.

In the same field of endeavor, Peace discloses: serial data (first and second serial data)(column 4, lines 65-67 through column 5, line 1).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Peace so that independent serial data (first and second serial data) from the T1/E1 data connections are received the rationale being serial data requires less transmit/reception connections (compared to parallel data)).

In the field of clock selection used for data transmission, Hashiguchi teaches a plurality of clock based functionalities, using a selected clock, for subsequent processing of serial data (Fig. 4, block 16 “output clock selector”, and blocks 13-1,13-2, 13-3, these correspond to a plurality of clock based functionalities, see signal UyCHT, (y=is 2,3,4 for the 13-1, 13-2, 13-3 respectively) requesting a transmit clock, supplied to them by the output clock selector, see column 2, lines 56-67 through column 3, lines 1-3, where the requested clock routed to the clock based functionality corresponds to a selected clock signal).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Hashiguchi so that a plurality of clock based functionalities choose among the first recovered clock, the second recovered clock, and the reference clock for subsequent processing of one of the first serial data and the second serial data, so that active lines are internally clocked (using a clock having a highest priority Mahajan et al. column 3, lines 44-50) to various modules within the access server where the data is analyzed and routed (Mahajan et al. column 1, lines 22-24).

With respect to claim 4, the system of Mahajan et al. modified by Peace and Hashiguchi further includes: wherein the first serial data is an receive serial bit stream (Fig. 2, T1 is a received serial bit stream).

With respect to claim 5, the system of Mahajan et al. modified by Peace and Hashiguchi further includes: wherein the plurality of clock based functionalities comprises a portion of a programmable logic fabric (see column 1, lines 19-24, and column 3, lines 44-50 and Fig. 2, where the user configuration commands supplied from the user interface, render the system of Mahajan et al. a programmable logic fabric).

With respect to claim 6, Mahajan et al. disclose: first circuitry for receiving first data and recovering a first recovered clock based on the first data (Fig. 2 see block 210, receiving data T1 and outputting recovered clock signal CLK1, see column 4, lines 12-22); wherein the first circuitry provides the first recovered clock to a logic fabric comprising a first clock based functionality (Fig. 2 see CLK1 is supplied to DMUX 254 of block logic fabric 250, comprising blocks 252, 254 and the data switch (that used the selected clock but is not shown in Fig.2) column 2, lines 58-65) and second circuitry for generating and providing a reference clock to the logic fabric (Fig. 2 see clock signal osc, corresponds to the reference clock, source of this clock is a free running oscillator, see column 1, lines 59-60); third circuitry for receiving second data and recovering a second recovered clock based on the second data (Fig. 2, block 220 CLK2 is the recovered clock column 4, lines 12-22); wherein the third circuitry provides the second

recovered clock to the logic fabric (see Fig. 2, CLK2 is supplied to block 250); wherein the first clock based functionality performs processing functions by choosing among the first recovered clock, the second recovered clock, and the reference clock (column 1, lines 58-65, the selected clock is used for subsequent processing, as a data transfer clock for example).

Mahajan et al. do not expressly teach: serial data. Furthermore the difference between Mahajan et al. and claim 6 is that Mahajan et al. teaches one clock based functionality compared to the claimed multiple clock based functionalities (three clock based functionalities) each concurrently performs processing functions by choosing among the first recovered clock, the second recovered clock, and the reference clock.

In the same field of endeavor, Peace discloses: serial data (first and second serial data)(column 4, lines 65-67 through column 5, line 1).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Peace so that independent serial data (first and second serial data) from the T1/E1 data connections are received the rationale being serial data requires less transmit/reception connections (compared to parallel data)).

In the field of clock selection used for data transmission, Hashiguchi teaches a plurality of clock based functionalities concurrently performing processing functions, using a selected clock, (Fig. 4, block 16 “output clock selector”, and blocks 13-1,13-2, 13-3, these correspond to a plurality of clock based functionalities, see signal UyCHT, (y=is 2,3,4 for the 13-1, 13-2, 13-3 respectively) requesting a transmit clock, supplied to

them by the output clock selector, see column 2, lines 56-67 through column 3, lines 1-3, column 6, lines 52-60, where the requested clock routed to the clock based functionality corresponds to a selected clock signal, and with respect to the concurrent performing of processing functions by the clock based functionalities, see Fig. 4, case where concurrent clock request signals are supplied into block 17, and concurrent supply of the requested clock signals to blocks 13-1, 13-2, 13-3 (for example) used for concurrent processing (serial transmission)).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Hashiguchi so that each of the first, second, and third clock based functionalities concurrently perform processing functions, by choosing among the fist recovered clock, the second recovered clock, and the reference clock, so that active lines are internally clocked (using a clock having a highest priority Mahajan et al. column 3, lines 44-50) to various modules concurrently within the access server where the data is analyzed and routed (Mahajan et al. column 1, lines 22-24 so that concurrent processing functions take place, i.e. parallel processing which is less time consuming).

With respect to claim 19, claim 19 is rejected based on a rationale similar to the one used to reject claim 10 above.

With respect to claim 20, the system obtained by modifying Mahajan et al. based on Peace and Hashiguchi further disclose: wherein the first serial bit stream is a receive

serial bit stream (Fig. 2 T1 is received by block 210 of the access network, i.e. is a receive serial bit stream).

With respect to claim 21, the system obtained by modifying Mahajan et al. based on Peace and Hashiguchi further disclose: wherein the second serial bit stream is a transmit serial bit stream (Fig. 2 T2 is a transmit serial bit stream for the transmitter when it originated).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahajan et al. (U.S. 6,618,358) in view of Peace (U.S. 6,687,260) and Hashiguchi (U.S. 5,987,540), as applied to claim 1, and further in view of Tang et al. (U.S. 2002/0075981).

With respect to claim 3, all of the limitations of claim 3 are rejected above in the rejection of claim 1, but neither Mahajan et al. nor Peace or Hashiguchi expressly teach: delay locked loop circuitry for receiving second serial data and produces a second recovered clock form the second serial data.

In the same field of endeavor (processing serial data and CDR) Tang et. al., disclose: delay locked loop circuitry (see Fig. 7, 703 clock recovery DLL, part of dual loop retimer see paragraphs [0036]-[0041]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of teachings of Tang et al., so that the clock recovery circuit of Mahajan et al.

comprises a delay-locked loop circuit, (such as the clock recovery system of Tang et. al.) that has minimum jitter generation and maximum jitter suppression (Tang et al., [0013] and [0041]).

6. Claims 10-12, 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahajan et al. (U.S. 6,618,358) in view of Hashiguchi (U.S. 5,987,540).

With respect to claim 10, Mahajan et al. disclose: at least one clock recovery circuitry coupled to receive a high data rate input data stream(Fig. 2 see block s 210, 220 etc receiving high speed data rate inputs T1 , T2 …Tn and outputting recovered clock signals CLK1, CLK2, CLKn see column 4, lines 12-22);wherein the clock recovery circuitry recovers a plurality of recovered clocks based on the high data rate input data stream (column 4, lines 20-21); a programmable logic fabric portion comprising a clock based functionality (Fig. 2, block 250, clock based functionality comprises blocks 252, 254 and the not shown TDM switch for example, see column 1, lines 62-65), wherein the clock based functionality performs subsequent processing by choosing among the plurality of recovered clocks, and a reference clock (column 1, lines 58-65, the subsequent processing is performed based on the selected clock signal).

Mahajan et al. do not expressly teach: a plurality of clock based functionalities; wherein each of the clock based functionalities performs subsequent processing by choosing among the plurality of recovered clocks and a reference clocks.

In the field of clock selection used for data transmission, Hashiguchi teaches a plurality of clock based functionalities, using a selected clock, for subsequent

processing of serial data (Fig. 4, block 16 “output clock selector”, and blocks 13-1,13-2, 13-3, these correspond to a plurality of clock based functionalities, see signal UyCHT, (y=is 2,3,4 for the 13-1, 13-2, 13-3 respectively) requesting a transmit clock, supplied to them by the output clock selector, see column 2, lines 56-67 through column 3, lines 1-3, where the requested clock routed to the clock based functionality corresponds to a selected clock signal).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Hashiguchi so that a plurality of clock based functionalities choose among the first recovered clock, the second recovered clock, and the reference clock for subsequent processing, so that active lines are internally clocked (using a clock having a highest priority Mahajan et al. column 3, lines 44-50) to various modules within the access server where the data is analyzed and routed (Mahajan et al. column 1, lines 22-24).

With respect to claim 11, Mahajan et al. disclose: wherein the high data rate input data stream is received according to a first protocol and is converted to a second protocol by the programmable logic fabric portion based on one of said plurality of recovered clocks (Fig. 2 received data stream are T1/E1 type data streams, column 1, lines 19-25, 62-65, the access server functions receives/transmits data , functions as a switch, and converts the active data to a TDM data stream).

With respect to claim 12, Mahajan et al. disclose: further comprising transmit circuitry coupled to receive the converted high rate input data stream in the second protocol, wherein the programmable logic fabric portion provides the converted high data rate input data stream in the second protocol based on one of said plurality of recovered clocks (column 1, lines 19-25, 62-65, the TDM switch used for internal routing (transmission) of the data, based on the selected clock).

Claim 22 is rejected based on a rationale similar to the one used to reject claim 6 above.

With respect to claim 23, Mahajan et al. disclose: receiving a plurality of input data streams (Fig. 2, see T1 signals received by blocks 210, 220, 230); recovering a corresponding plurality of clocks based on the plurality of input data streams)Fig. 2, blocks 210, 220, 230 recover clock signals CLK1…CLKn from the plurality of input data streams see column 4, lines 16-21);determining at least one output port for providing outgoing data streams; and providing input streams to the at least one output port by choosing among the plurality of recovered clocks (see column 1, lines 19-26, 59-65, where data is routed (transmitted) using a data switch to various modules and this corresponds to the claimed determining step, that determines output ports for providing outgoing data streams).

Mahajan et al. do not expressly teach: providing each input data stream of the plurality of input data streams to the at least one output port by choosing among the

plurality of recovered clocks; wherein the at least one output port comprises a number of output ports that corresponds to a number of input streams, and wherein the method comprises further determining, for each input data stream of the plurality of input data streams, an output port and providing each input data stream of the plurality of input data streams to the determined output ports based upon a chosen one of the plurality of recovered clocks.

In the field of clock selection used for data transmission, Hashiguchi discloses: (Fig. 4, block 16 “output clock selector”, and blocks 13-1,13-2, 13-3, 14-1, 14-2, 14-3 these correspond to a plurality of transmitting and receiving ports, and each of 13-1,13-2, 13-3 requests a transmit clock that is supplied to them by the output clock selector, see column 2, lines 56-67 through column 3, lines 1-3, to transmit respective serial data).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Hashiguchi so that each input data stream (the T1 data streams of Mahajan et al.) are provided to an output port, by choosing (i.e. based on) the selected clock signal from the plurality of recovered clocks.

The system obtained by modifying Mahajan et al. based on the teachings of Hashiguchi comprises a number of output ports that correspond to a number of data input streams and with respect to the determining step, i.e. the determining for each input data stream of the plurality of input data streams, an output port, see Mahajan et al. (column 1, lines 22-24, see that the data is routed to various modules).

7. Claim 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahajan et al. (U.S. 6,618,358) in view of Hashiguchi (U.S. 5,987,540) as applied to claim 10 above, and further in view of Peace (U.S. 6,687,260).

With respect to claim 13, all of the limitations of claim 13 are rejected below, and Mahajan et al. disclose: wherein said at least one clock recovery circuit comprises a second clock recovery circuit for recovering a second recovered clock based on an I/O data stream (Fig. 2, see block 220 recovering CLK2 for second data stream). Neither Mahajan et al. nor Hashiguchi expressly teach: serial data stream.

In the same field of endeavor, Peace discloses: serial data (first and second serial data)(column 4, lines 65-67 through column 5, line 1).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Peace so that independent serial data (first and second serial data) from the T1/E1 data connections are received the rationale being serial data requires less transmit/reception connections (compared to parallel data)).

8. Claims 14-16, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahajan et al. (U.S. 6,618,358) in view of Hashiguchi (U.S. 5,987,540) and Mann et al. (U.S. 5,251,210).

Claim 14 is rejected based on a rationale similar to the one used to reject claim 10 above. However, neither Mahajan et al. nor Hashiguchi expressly teach: recovering a second recovered clock based on a transmitter clock.

In the same field of endeavor, Mann et al. disclose: recovering a second recovered clock based on a transmitter clock (Fig. 7, second clock recovered from Channel 2 data, and see Fig. 5, where transmitter uses a transmitter clock (block 110) to generate the Channel 2 data i.e. clock recovery at the receiver is based on a transmitter clock used to transmit the data stream).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Mann so that the clock recovery at the receiver is based on the received data (i.e. indirectly based on a transmitter clock) so that that an embedded clock is extracted for the received data (i.e. there is no need to transmit a separate clock signal in addition to the data signal).

With respect to claim 15, Mahajan et al. further disclose: wherein the high data rate input data stream is received according to a first protocol (Fig. 2, see T1/E1 input data).

With respect to claim 16, Mahajan et al. further disclose: wherein the high data rate input data stream is converted to a second protocol based on the first recovered clock (see column 1, lines 19-30, 60-65, where data is clocked in a TDM fashion based on the highest priority clock signal, for example the first recovered clock).

With respect to claim18, Mahajan et al. further disclose: further comprising transmitting the converted high data rate input data stream in the second protocol based on the second recovered clock (column 1, lines 19-30, 60-65).

9. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahajan et al. (U.S. 6,618,358) in view of Peace (U.S. 6,687,260) and Ohtsuka (U.S. 5,388,100).

With respect to claim 8, Mahajan et al. disclose: circuitry for receiving input data streams (Fig. 2, block 250 and blocks 210, 220, 230, receive T1 streams of data);clock recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams (Fig. 2, blocks 210, 220, 230, recover clocks from respective input data streams, column 4, lines 16-21); circuitry for providing a reference clock (Fig. 2, osc, reference clock signal is output form an oscillator generating circuit, column1, lines 55-57); logic that provides data to an outgoing transmit block by choosing from among the plurality of recovered clocks and said reference clock (see column 1, lines 59-65, where the selected clock is used to clock a data switch (outgoing transmit block) used for routing data, see column 1, lines 19-24).

Mahajan et al. do not expressly teach: serial data streams; logic for selecting from the plurality of input serial streams and for providing at least one outgoing serial data stream to an outgoing transmit block; wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing

transmit block by choosing from among the plurality of recovered clocks and said reference clock.

In the same field of endeavor, Peace discloses: serial data streams (column 4, lines 65-67 through column 5, line 1).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Peace so that independent serial data streams from the T1/E1 data connections are received the rationale being serial data requires less transmit/reception connections (compared to parallel data)).

In the field of data selection, Ohtsuka discloses: logic for selecting from a plurality of serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block (Fig. 2, see plurality of serial data streams D11, D12, D13, D14 and selector 52, see column 3, lines 21-30,see the mentioned the bit serial data) supplied to logic for selecting and for providing at least one outgoing serial streams to an outgoing transmit block (selector 52, and the received data is supplied (transmitted) to a circuit that follows (column 3, lines 54-55); wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block (Fig. 3, each of the D11, D12, D13, D14 is selected and provides in a TDM fashion to the circuit that follows).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mahajan et al. based on the teachings of Ohtsuka,

so that the input data streams are processed in a time-division manner for the purpose of efficient use of time (Ohtsuka column 1, lines 18-25).

With respect to claim 9, Mahajan et al. further discloses: wherein the outgoing transmit block is one of a programmable transmit physical media attachment (PMA) module and a transmitter port (transmitter port, column 1, lines 62-65, where data in a data switch is understood to be output (transmitted) from a port).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SOPHIA VLAHOS/
Examiner, Art Unit 2611
8/20/2008

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611